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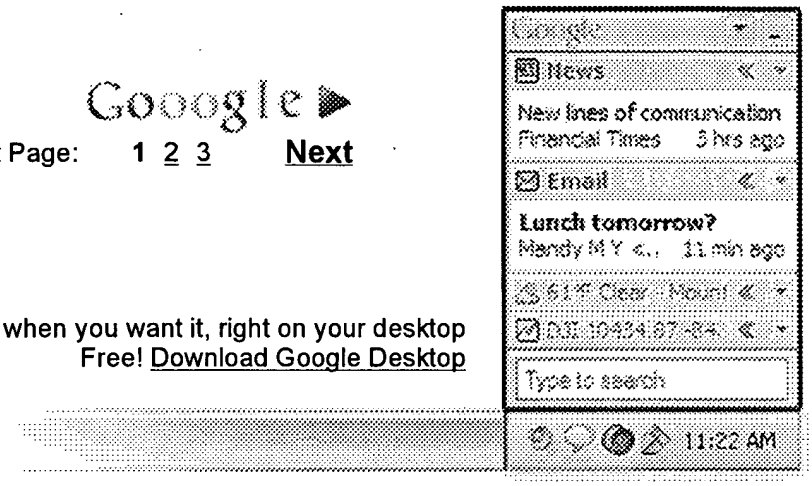
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1 High level specification and design: Achieving maximum performance: a method for the verification of interlocked pipeline control logic
Kerstin Eder, Geoff Barrett
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Publisher: ACM Press
Full text available: pdf(82.28 KB) Additional Information: full citation, abstract, references, index terms

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Keywords: interlock logic, pipeline stall, verification

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Publisher: ACM Press
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Keywords: abstraction mappings, cache coherence protocols, distributed systems, finite state machines, model checking, verification

5 Advances in accelerated simulation: A fast hardware/software co-verification method for system-on-a-chip by using a C/C++ simulator and FPGA emulator with shared register communication
Yuichi Nakamura, Kouhei Hosokawa, Ichiro Kuroda, Ko Yoshikawa, Takeshi Yoshimura
June 2004 **Proceedings of the 41st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, index terms

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Keywords: C/C++ simulator, FPGA emulation, co-verification

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Jing Dong
November 2000 **Proceedings of the 2000 conference of the Centre for Advanced Studies on Collaborative research**
Publisher: IBM Press
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7 Moving towards more effective validation: A comparison of three verification techniques: directed testing, pseudo-random testing and property checking
Mike G. Bartley, Darren Galpin, Tim Blackmore
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Murali Kudlugi, Soha Hassoun, Charles Selvidge, Duaine Pryor
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Publisher: ACM Press

Full text available: pdf(201.24 KB) Additional Information: full citation, abstract, references, citings, index terms

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9 Formal verification of iterative algorithms in microprocessors

Mark D. Aagaard, Robert B. Jones, Roope Kaivola, Katherine R. Kohatsu, Carl-Johan H. Seger
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(81.11 KB) Additional Information: full citation, abstract, references, citings, index terms

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Keywords: HW/SW co-design, HW/SW co-verification, RTC, emulation, system modeling, virtual components

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Keywords: fast prototyping, hardware/software (HW/SW) co-design, system design, system modeling, system verification, virtual component (VC) re-use

14 A reconfigurable logic machine for fast event-driven simulation
Jerry Bauer, Michael Bershteyn, Ian Kaplan, Paul Vyedin
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(129.52 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

As the density of VLSI circuits increases, software techniques cannot effectively simulate designs through the millions of simulation cycles needed for verification. Emulation can supply the necessary capacity and performance, but emulation is limited to designs that are structural or can be synthesized. This paper discusses a new system architecture that dramatically accelerates event-driven behavioral simulation and describes how it is merged with emulation.

Keywords: event-driven simulation, reconfigurable computing

15 Virtual chip: making functional models work on real target systems
Namseung Kim, Hoon Choi, Seungjong Lee, Seungwang Lee, In-Cheolo Park, Chong-Min Kyung
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(254.01 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

As design complexity increases, functional verification becomes a crucial issue to ensure design correctness at an early design stage. Traditional methods for verifying functional designs are based on the HDL simulation, which is becoming the bottleneck of the design cycle because of the increasing design complexity. The accurate verification ability at the architectural level through a large set of the test programs and real world applications is a foundation for the next design step. In t ...

Keywords: emulation, functional simulation, reconstruction, visibility

16 High-level design verification of microprocessors via error modeling

D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, R. B. Brown

October 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 4

Publisher: ACM Press

Full text available: pdf(174.30 KB) Additional Information: full citation, abstract, references, citings, index terms

A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented. We have systematically collected design error data from a number of microprocessor design projects. The error data is used to derive error models suitable for design verification testing. A class of basic error models is identified and shown to yield tests that provide good coverage of comm ...

Keywords: design errors, design verification, error modeling

17 Observations on industrial practice using formal methods

Susan Gerhart, Dan Craigen, Ted Ralston

May 1993 **Proceedings of the 15th international conference on Software Engineering**

Publisher: IEEE Computer Society Press

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18 The formal verification of a pipelined double-precision IEEE floating-point multiplier

Mark D. Aagaard, Carl-Johan H. Seger

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(47.36 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Floating-point circuits are notoriously difficult to design and verify. For verification, simulation barely offers adequate coverage, conventional model-checking techniques are infeasible, and theorem-proving based verification is not sufficiently mature. In this paper we present the formal verification of a radix-eight, pipelined, IEEE double-precision floating-point multiplier. The verification was carried out using a mixture of model-checking and theorem-proving techniques in the Voss hardwar ...

Keywords: Hardware verification, floating-point arithmetic, ANSI/IEEE Std 754-1985, model checking, theorem proving

19 A formal definition of priority in CSP

C. J. Fidge

September 1993 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 15 Issue 4

Publisher: ACM Press

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, index terms, review

The process models of Ada and occam are formally based on the CSP process algebra. However, for fine-tuning real-time performance, they include "prioritized" constructs that have no counterparts in CSP. These constructs therefore lack any formal definition, a

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Keywords: Ada, Communicating Sequential Processes, Priority, occam, real-time programming

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A design verification methodology for microprocessor hardware based on modeling design errors and generating simulation vectors for the modeled errors via physical fault testing techniques is presented. We have systematically collected design error data from a number of microprocessor design projects. The error data is used to derive error models suitable for design verification testing. A class of basic error models is identified and shown to yield tests that provide good coverage of comm ...

Keywords: design errors, design verification, error modeling

17 Observations on industrial practice using formal methods

Susan Gerhart, Dan Craigen, Ted Ralston

May 1993 **Proceedings of the 15th international conference on Software Engineering**

Publisher: IEEE Computer Society Press

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18 The formal verification of a pipelined double-precision IEEE floating-point multiplier

Mark D. Aagaard, Carl-Johan H. Seger

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(47.36 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Floating-point circuits are notoriously difficult to design and verify. For verification, simulation barely offers adequate coverage, conventional model-checking techniques are infeasible, and theorem-proving based verification is not sufficiently mature. In this paper we present the formal verification of a radix-eight, pipelined, IEEE double-precision floating-point multiplier. The verification was carried out using a mixture of model-checking and theorem-proving techniques in the Voss hardwar ...

Keywords: Hardware verification, floating-point arithmetic, ANSI/IEEE Std 754-1985, model checking, theorem proving

19 A formal definition of priority in CSP

C. J. Fidge

September 1993 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 15 Issue 4

Publisher: ACM Press

Full text available: pdf(1.37 MB) Additional Information: full citation, abstract, references, index terms, review

The process models of Ada and occam are formally based on the CSP process algebra. However, for fine-tuning real-time performance, they include "prioritized" constructs that have no counterparts in CSP. These constructs therefore lack any formal definition, a

situation that leaves room for misunderstandings. We extend CSP with a formal definition of the notion of priority. The definition is then used to assess the transputer implementation of priority in occam and the definition ...

Keywords: Ada, Communicating Sequential Processes, Priority, occam, real-time programming

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